CLAIMS

What is claimed is:

1. An apparatus, comprising:

a first interface;

a second interface not directly coupled to said first interface; and

a cache accessible from said first interface and said second interface, to contain a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface.

2. The apparatus of claim 1, wherein said first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor.

3. The apparatus of claim 2, wherein said second cache coherency state is to reduce snoop transactions on said second interface.

4. The apparatus of claim 2, wherein said first cache coherency state is exclusive and said second cache coherency state is shared.

5. The apparatus of claim 2, wherein said first cache coherency state is modified and said second cache coherency state is shared.

6. The apparatus of claim 3, wherein said second cache coherency state supports speculative invalidation.

7. The apparatus of claim 6, wherein said first cache coherency state is modified and said second cache coherency state is invalid.

8. The apparatus of claim 6, wherein said first cache coherency state is exclusive and said second cache coherency state is invalid.

9. The apparatus of claim 6, wherein said first cache coherency state is shared and said second cache coherency state is invalid.

10. The apparatus of claim 6, wherein said second cache coherency state further supports explicit invalidation.

11. A method, comprising:

associating a first cache coherency state with a first cache line in a first cache;

associating a second cache coherency state with a second cache line in a second cache in an inner relationship to said first cache;

transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces; and

transitioning said second cache coherency state to said third cache coherency state.

12. The method of claim 11, wherein said first cache coherency state is exclusive, said second cache coherency state is invalid, and said third cache coherency state is shared.

13. The method of claim 11, wherein said first cache coherency state is modified, said second cache coherency state is modified, and said third cache coherency state is invalid.

14. A method, comprising:

associating a first cache coherency state with a first cache line in a first cache;

associating a second cache coherency state with a second cache line in a second cache in an inner relationship to said first cache;

transitioning said second cache coherency state to an invalid state; and

transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for outer interfaces and an invalid state for inner interfaces.

15. The method of claim 14, wherein said first cache coherency state is modified.

16. The method of claim 14, wherein said first cache coherency state is exclusive.

17. The method of claim 14, wherein said first cache coherency state is shared.

18. A method, comprising:

associating a first cache coherency state with a first cache line in a first cache;

associating an invalid state with a second cache line in a second cache in an inner relationship to said first cache;

transitioning said invalid state to a shared state; and

transitioning said first cache coherency state to a joint cache coherency state including a shared state for inner interfaces.

19. The method of claim 18, wherein said first cache coherency state is invalid and said joint cache coherency state is exclusive-shared.

20. The method of claim 18, wherein said first cache coherency state is modified-invalid and said joint cache coherency state is modified-shared.

21. An apparatus, comprising:

means for associating a first cache coherency state with a first cache line in a first cache;

means for associating a second cache coherency state with a second cache line in a second cache in an inner relationship to said first cache;

means for transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces; and

means for transitioning said second cache coherency state to said third cache coherency state.

22. The apparatus of claim 21, wherein said first cache coherency state is exclusive, said second cache coherency state is invalid, and said third cache coherency state is shared.

23. The apparatus of claim 21, wherein said first cache coherency state is modified, said second cache coherency state is modified, and said third cache coherency state is invalid.

24. An apparatus, comprising:

means for associating a first cache coherency state with a first cache line in a first cache;

means for associating a second cache coherency state with a second cache line in a second cache in an inner relationship to said first cache;

means for transitioning said second cache coherency state to an invalid state; and

means for transitioning said first cache coherency state to a joint cache coherency state including said first cache coherency state for outer interfaces and an invalid state for inner interfaces.

25. The method of claim 24, wherein said first cache coherency state is modified.

26. The method of claim 24, wherein said first cache coherency state is exclusive.

27. The method of claim 24, wherein said first cache coherency state is shared.

28. An apparatus, comprising:

means for associating a first cache coherency state with a first cache line in a first cache;

means for associating an invalid state with a second cache line in a second cache in an inner relationship to said first cache;

means for transitioning said invalid state to a shared state; and

means for transitioning said first cache coherency state to a joint cache coherency state including a shared state for inner interfaces.

29. The apparatus of claim 28, wherein said first cache coherency state is invalid and said joint cache coherency state is exclusive-shared.

30. The apparatus of claim 28, wherein said first cache coherency state is modified-invalid and said joint cache coherency state is modified-shared.

31. A system, comprising:

a cache accessible from a first interface and a second interface, to contain a cache line with a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface;

a bus bridge to a third interface; and

an input-output device coupled to said third interface.

32. The system of claim 31, wherein said first cache coherency state has higher privilege than said second cache coherency state when said second interface is coupled to a processor.

33. The system of claim 31, wherein said second cache coherency state is to reduce snoop transactions on said second interface.